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An Integrated CMOS Bio-potential Amplifier with a Feed-Forward DC Cancellation Topology

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***Abstract*—This paper describes a novel technique to realize an integrated CMOS bio-potential amplifier with a feed-forward DC cancellation topology. The amplifier is designed to provide substantial DC cancellation even while amplifying very low frequency signals. More than 80dB Offset Rejection Ratio is achieved without any external capacitors. The cancellation scheme is robust against process and temperature variations. The amplifier is fabricated through MOSIS AMI 1.5µm technology (0.05mm^2 area). Measurement results show a gain of 43.5dB in the pass band (<1mHz-5KHz), an input referred noise of 3.66µVrms, and a current consumption of 22µA.**

I. INTRODUCTION

A critical problem facing integrated bio-potential amplifier designers is that of the DC-offset cancellation. This offset (100-500mV) is created at the electrode-electrolyte interface and is typically many times (occasionally up to 1000 times) greater than the signal voltage to be measured (e.g., 100-500µV extracellular potentials) [1]. Without adequate attenuation, this offset easily saturates the input stage amplifiers. In discrete implementations, one can easily achieve a low cutoff frequency by using an off-the-shelf capacitor. However, if one desires to integrate such amplifiers (e.g., in applications such as implantable multichannel neural recording systems), the real estate consumed by such large capacitors is usually prohibitive. Over the years many techniques have been proposed to attenuate the offset and provide a high gain in the pass band. Some of these use capacitors in conjunction with large resistors ($10^{12}\Omega$ range using MOSFETS) to block the DC; others use various loading and feedback techniques to suppress the offset [1-8]. The primary drawback of many of these methods is that they are not suitable for amplifying local field potentials (1-300Hz). Table 1 compares some important performance parameters of these bio-potential amplifiers. In order to gain a better understanding of the amount of rejection, we introduce a new metric called Offset Rejection Ratio (ORR). ORR is defined as the ratio of the pass-band gain to the DC-offset rejection at the output of the amplifier.

Our unique topology needs no additional capacitor yet provides a substantial DC-offset cancellation while amplifying Local Field Potentials and unit action potentials (300-5000Hz). The amplifier is also optimized for low power and low noise. Even though the technique in [1, 2, 3] allows for Local Field Potential recordings, the pass-band gain is set by the ratio of capacitors that consume the bulk of the area.

TABLE I
SUMMARY OF THE PERFORMANCE OF REPORTED NEURAL RECORDING AMPLIFIERS

	BW (Hz)	ORR (dB)	Noise (µVrms)	Area (mm^2)	Current (µA)
[1]	10-7.3K	AC coupled 44dB gain	9	-	10
[2]	1-9.9K	AC coupled 40dB gain	9.2	0.177	22.6
[3]	<1m-7.2K	AC coupled 40dB gain	2.2	0.16	16
[4]	15-7K	50	15	0.07	60
[5]	100-3.2K	50	12	0.2	60
[6]	20-75K	71	-	0.18	50
[7]	100-10K	Buffer + AC gain	11	Multi-stage	-
[8]	211-5K	47.4	4.4	External caps	200
[9]	50-9.1K	70	7.8	0.107	37
This work	<1m -5K	81.5	3.66	0.05	22

II. AMPLIFIER DESIGN AND SIMULATION

II.A. Feed-forward DC cancellation technique

In our technique, the input signal passes through two paths designed such that the amplitude and phase characteristics through either are the same for DC but different for the desired signal (ω_s). Hence by subtracting their outputs, DC would cancel itself while the signal would not. To realize the above principle, the input DC and signal (ω_s) are filtered through a first-order low pass filter with cutoff frequency of ω_s. The output of the filter is then subtracted from its input. Since the low pass filter passes DC but attenuates ω_s, on subtraction with its input, DC is

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cancelled. The subtracting block is also designed to amplify the signal. The block diagram of the proposed amplifier is shown in Fig. 1. The frequency spectrum representation of the signal (ω_s) and the DC-offset through various points marked (A, B, C) in the amplifier is illustrated in Fig. 2. The transfer function of the amplifier is given by

$$H(s) = \frac{Y(s)}{U(s)} = \frac{-Gs}{s+1} \quad (1)$$

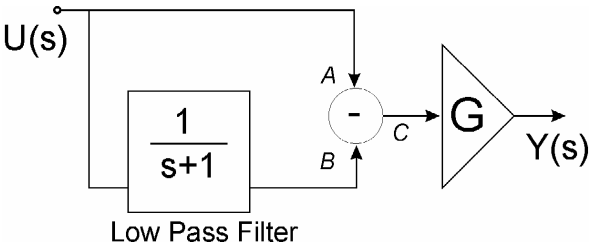

Fig.1. Block diagram of the feed-forward DC reject amplifier

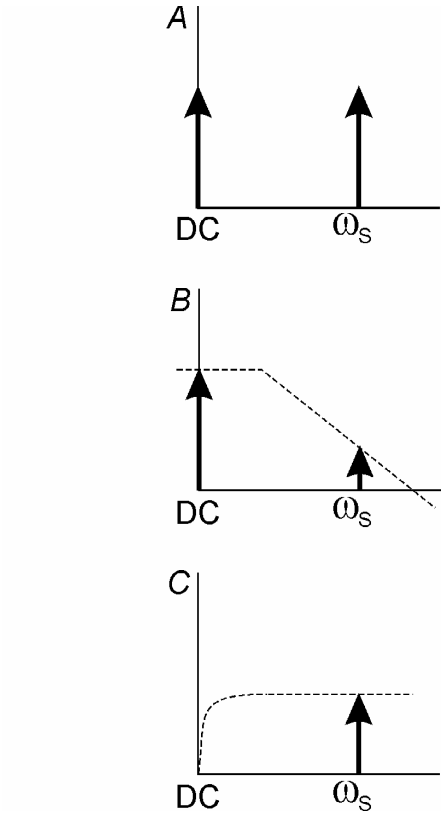

Fig.2. Illustrations showing the path of the DC and the signal of interest (ωs) through the various nodes (A, B, C) in the amplifier.

II.B. Integrated bio-potential amplifier

A CMOS integrated bio-potential amplifier based on the above concept was realized as shown in Figs. 3, 4. The subtraction block was realized using an Operational Transconductance Amplifier (OTA). The input capacitance of the OTA (typically ~1pF) and a MOS-bipolar pseudo-resistor (10^{14}-$10^{16}\Omega$) were used to generate the low frequency pole – thereby eliminating the need for any external capacitor. Standard design techniques were followed so that the OTA met low power, low noise requirements [3]. It is important to note that the overall DC rejection technique is not affected by the choices made to design the OTA. A suitable Operational Amplifier could substitute the OTA if the circuit is driving resistive loads.

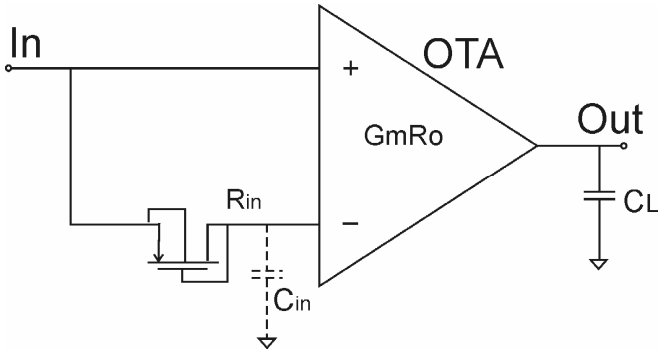

Fig. 3. Block diagram of proposed integrated neural amplifier.

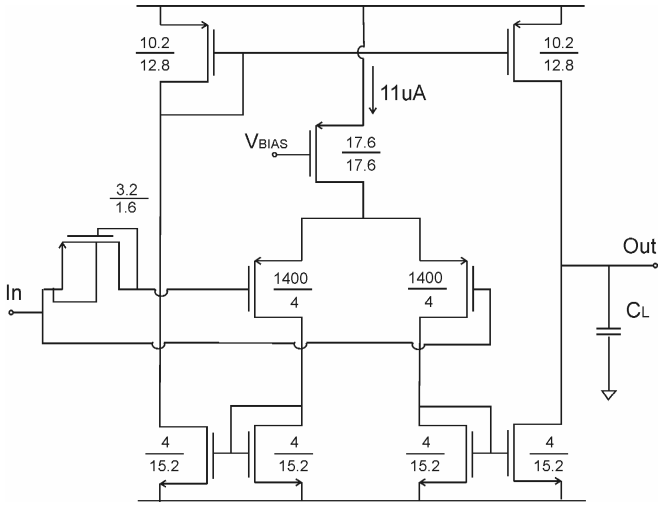

Fig. 4. Schematic of the proposed neural amplifier.

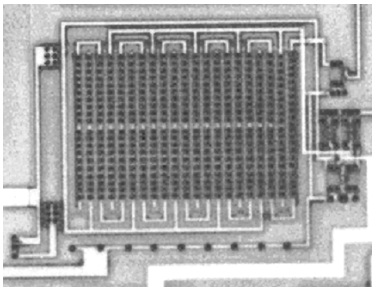

Fig.5. Die micrograph of neural amplifier fabricated using AMI 1.5µ CMOS process (fabricated at MOSIS - CA, USA)

II.C. Effect of process and temperature variations

Fig. 6 shows the simulation results of the effect of pole location variation (due to either resistance or input capacitance value variance) on the transfer function of the neural amplifier. As observed, even if the resistance of the pseudo-resistor shifts by two orders of magnitude (because of process or temperature variations), it would not affect the pass-band gain and the DC-offset rejection – this is an added advantage of this technique.

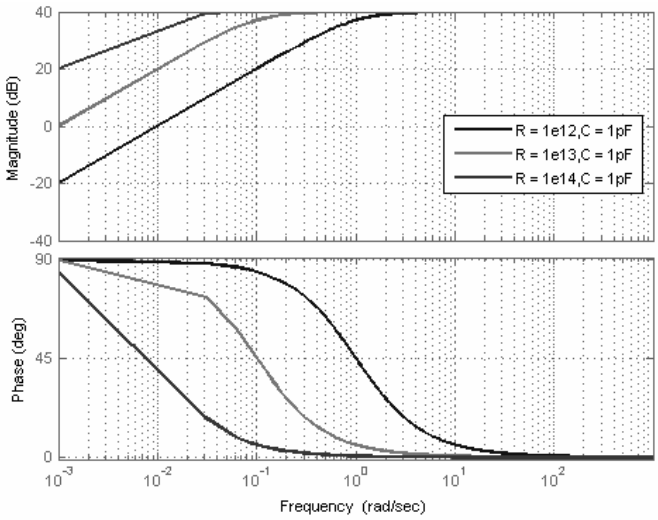

Fig. 6. Plot showing the effect of variation of resistance of the MOS resistor on the Transfer Function of the amplifier.

III. EXPERIMENTAL RESULTS

The following sections present the AC, DC, transient, and noise response of the amplifier.

III.A. DC characterization

The amplifier was fed a DC input in the range of ±1 V and the output was measured to measure the DC-offset rejection capability of the circuit, Fig. 7. As can be seen, the output Q-point shifts approximately ±13mV for a ±1 V input. This equates to a DC rejection of approximately -38 dB.

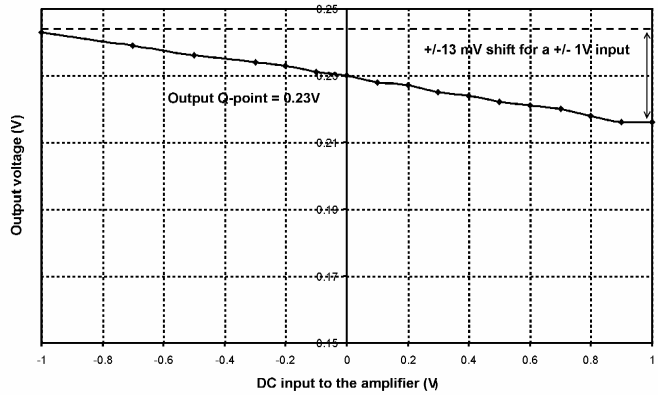

Fig.7. DC response of the amplifier. The amplifier can successfully reject more than 1V of DC input

III.B. AC characterization

The magnitude response of the amplifier was measured using a network analyzer capable of doing extreme low-frequency measurements (10mHz). Fig. 8 shows the measured (solid line) and simulated (dotted line) magnitude response of the amplifier. In the measurable range of the network analyzer, both results match very well. The amplifier exhibits a pass-band gain of 43.5dB with a bandwidth of <1mHz to 5KHz. The measured Offset Rejection Ratio for the amplifier is therefore 43.5dB + |-38 dB| = 81.5dB.

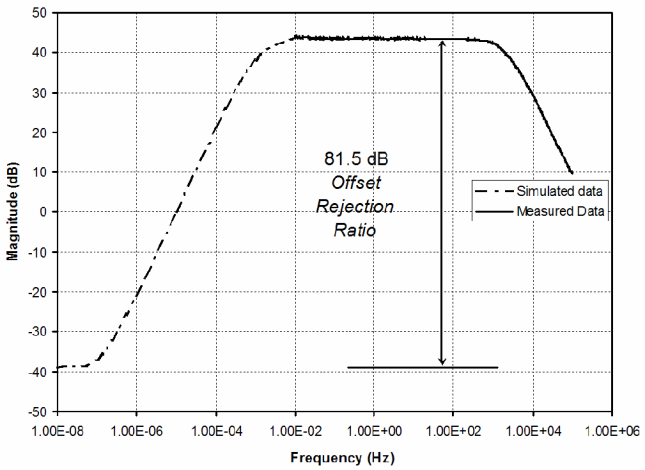

Fig. 8. AC response of the amplifier.

III.C. Transient response

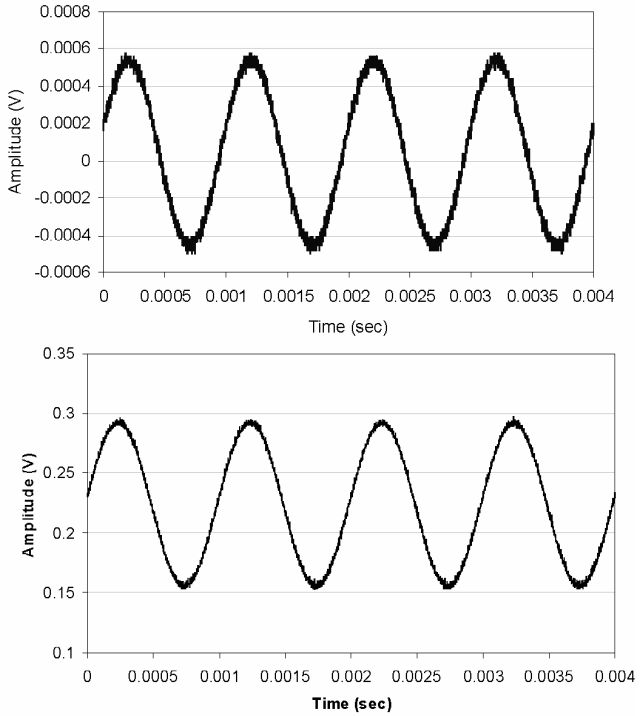

Fig.9. a) Plot showing the 1mVp-p, 1 KHz input to the amplifier, b) output of the amplifier.

A 1mVp-p input at 1KHz was fed to the amplifier and its output response was measured, Fig. 9-a, b. The circuit

amplified the input by approximately 150x. The output sinusoid also rode on a 0.23V DC signal. The output Q-point of 0.23V is due to the internal mismatches in the OTA. Future designs could incorporate circuitry to set the output Q-point even closer to 0V.

III.D. Noise performance

Fig. 10 shows a plot of the measured and simulated input referred noise. The total input referred noise for the amplifier (from 1Hz–10kHz) was 3.66uVrms.

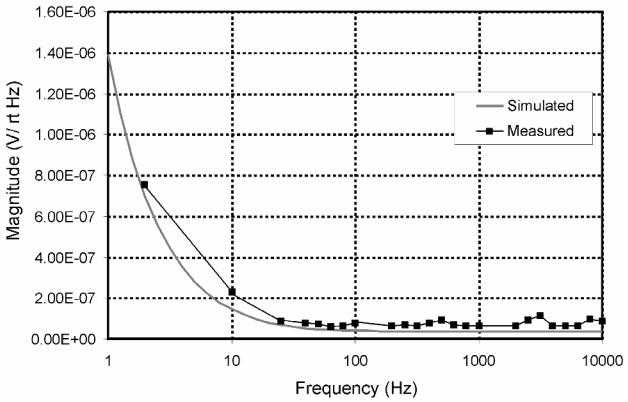

Fig.10. Measured and simulated input referred noise of the amplifier.

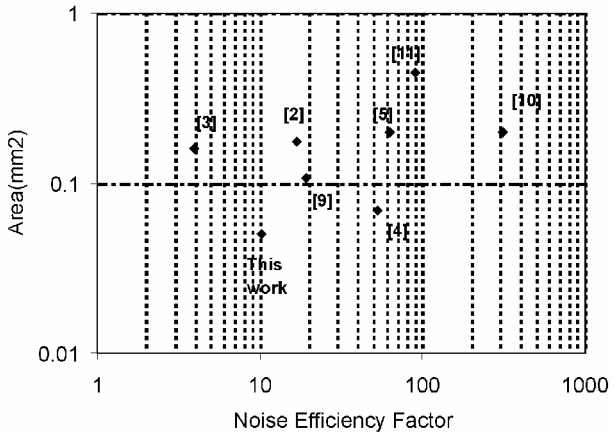

Fig. 11. Plot of NEF v/s Area consumed by each of the amplifiers.

A term introduced in [10], Noise Efficiency Factor (NEF), is a measure of the noise performance of a given amplifier as a function of its power consumption and the bandwidth.

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi.U_T.4kT.BW}} \qquad (2)$$

In equation (2), I_{tot} is the total current consumed by the amplifier, BW is its bandwidth, and $V_{ni,rms}$ is the RMS input referred noise voltage. In implantable multi-channel neural recording systems, apart from the noise performance, the amplifier area consumed is also critical. Fig. 12 shows the NEF v/s the area consumed by various reported amplifiers. It is clearly seen that the described amplifier achieves the best NEF-Area ratio.

IV. CONCLUSIONS

This work describes a feed-forward cancellation technique to realize an integrated DC-offset rejecting bio-potential amplifier. The amplifier provides substantial input DC-offset cancellation while amplifying very slow moving signals (> 1Hz). This amplifier *relies on subtracting the offset with itself rather than attenuating it using capacitors* and hence does not need any external capacitor*s*. The amplifier presents itself as an optimal candidate for use in multi-channel implanted neural recording circuits where integrated chip area and power consumption are important parameters. Simulation and measured results of the fabricated amplifier matched very well to provide > 80 dB of Offset Rejection Ratio.

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